Proc. Int. Symp. on Optical Memory, 1989
Japanese Journal of Applied Physics, Vol. 28 (1989) Supplement 28-3, pp.165-170

Improvement in Thermal Properties of a Multi-Beam Laser Diode Array

Setsuko MURATA and Kazutoshi NISHIMURA

NTT Applied Electronics Laboratories, 3-9-11, Midori-cho, Musashino-shi, Tokyo 180

(Received August 31, 1989)

Improvement in thermal performance of a high-density laser diode array including mutual thermal interactions is examined. Three-dimensional thermal analysis of a 50-μm-spaced 5-beam junction-down mounted *laser* diode array is performed on a practically scaled model, using the Boundary Element Method. The thermally dominant components are the chip and submount. The dominant heat flow route is also shown. A new structure is proposed that combines a high thermal conductive submount, a thin cap layer, and a heat-pass-wire, which acts as a bypass. This structure can almost halve the overall thermal resistance of conventionally structured laser arrays for 5-beam operations.

§1. Introduction

Achieving high data transfer rates is one of the most important goals of optical disk drive development. The rates are critically restricted by technical limits of the medium recording sensitivity, laser diode optical power, and disk rotation speed. A multi-beam laser diode array[1] has great potential to improve extremely high data transfer rates,[2,3] since it can simultaneously read or simultaneously write the closely spaced tracks by operating its laser diode elements in parallel. However, increasing the number of the laser elements increases outer element's beam signal degradation due to lens aberrations. Therefore, narrowing the element spacing is necessary.

It is well known that both operating characteristics and longevity of laser diodes are strongly affected by the junction temperature.[4] The junction temperature of a high-density laser diode array, which has many heat sources closely arranged on its substrate, increases more than that of a conventional single-beam laser diode because considerable mutual thermal interactions take place. Thus, improving the laser array thermal performance is very important.

The thermal analysis of a laser diode has been conducted by many researchers,[5-7] and improved performance has been achieved from the basic analysis by Joyce and Dixon.[8] In addition, laser array analysis has also been performed on the upper and lower thermal resistance bounds;[9] on the relationship between thermal resistance and the element spacing, using a special infinite element model;[10] and on heatsink design, especially for the phase locked operation;[11] and on heatsink design using a partial model.[12] However, improved thermal performance of a laser array has not yet been reported using a practically scaled full model.

This paper describes the improved thermal properties of a 50-μm-spaced 5-beam junction-down mounted laser diode array for high-speed optical disk drives, using a 3-dimensional practically scaled model. An analytic model using the Boundary Element Method[13] is shown in §2, and dominant thermal factors are investigated in §3. In factors and their effect are presented. The combined effect of these structures is discussed. A new structure is presented which has half the usual overall thermal resistance including mutual interactions.

§2. Analytic Model

Our model uses a 3-dimensional thermal analytic program called BEASY which is based on the Boundary Element Method. Figure 1 shows our laser array model. Heat flow symmetry about the Y-Z plane is used to simplify analysis, so the model represents half the full laser array. The model comprises four components: a laser chip, submount, heatsink and stem. Metal layers and solder contact layers are assumed to be negligible since they are relatively thin. The stem is a 9-mm diameter disk (a TO-5 transistor header), which is generally used to mount a laser diode. A cap is also used, the same as in a conventional laser diode, to seal the laser array hermetically and protect it from direct exposure to the air. However, because the contact area between the cap and the stem is relatively small and the cap is placed far from the heat source, heat conduction by the cap is assumed to be negligible. Therefore, the cap is omitted in the model. The two shaded planes in Fig. 1, which are the

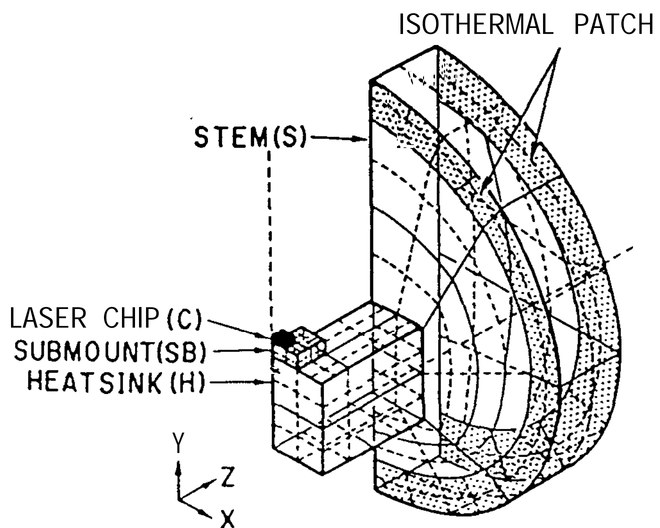

Table I. Parameters of a standard laser array model.

Component	Material	Thermal conductivity ($W \cdot mm^{-1} \cdot K^{-1}$)	Size (mm)
Laser Chip (C) (Heat Source)	GaAs (GaAlAs)	0.045 (0.016)	0.4x0.25x0.1 (0.004x0.25 x0.0001)
Submount (SB)	Si	0.168	1.2x0.7x0.3
Heatsink (H)	Cu	0.39	2.4x2.47x2.0
Stem (S)	Fe	0.0733	9φx1.5

outermost patches on each side of the stem, are assumed to be isothermal, since they contact an external high-conductive heatsink. The influences of heat radiation and convection are neglected because the laser is hermetically sealed by the cap and because most of the heat is conducted through the solid.

Table I lists materials, thermal conductivity, and the size of each component of a standard model. Temperature dependence of conductivity is neglected because the temperature rise is not significant. The standard submount material is conventional Si. The heat source is assumed to be a uniform rectangular volume source corresponding to a 4-μm-wide 250-μm-long 0. 1-pm-thick active region. A transformation is performed in the Y direction to simplify the laser chip model. This transformation replaces each epitaxial layer within the chip, except for the GaAlAs heat source, to a thermally equivalent GaAs layer.[14,15]

The laser chip model is shown in Fig. 2. The chip has 5 laser diode elements spaced at 50-μm intervals, with 4 etched grooves between the elements. These grooves electrically and optically isolate the elements for individual operation. The grooves are 10-μm wide and 10-μm deep. The chip is mounted on the submount with its junction down. This mounting is thermally superior to junction-up mounting, because the junction is nearer the submount. A layer between the heat source center and the chip surface facing the submount is defined as a cap layer. The standard model cap layer is 7-μm thick.

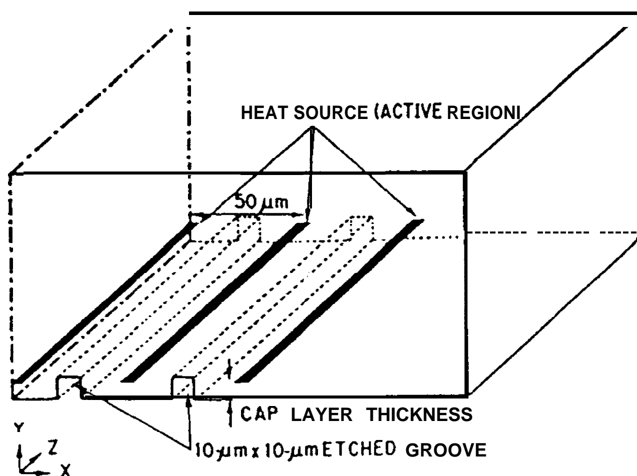

Fig. 2. Fifty-μm-spaced 5-beam junction-down mounted laser array chip structure.

It is assumed that all heat is generated only in the active region because this is the dominant heat area. The model is divided into up to 300 quadratic boundary elements, and more than half of these are used to divide the chip.

§3. Distribution of Thermal Resistance

To determine the thermally dominant factors, the following three items of the standard model are analyzed. First, the self thermal resist ante for single-element operation is divided into four model components. Second, the laser array's additional thermal resistance due to mutual thermal interaction among elements should be considered. Thus, the interactive thermal resistances for 50-μm- and 100-μm-spaced element operations are divided in the same manner. Last, the contributions of two different heat flow routes from the source to the self thermal resistance are examined.

3.1 *Self thermal resistance*

The self thermal resistance is divided into four model components to determine the thermally dominant components. First, the chip thermal resistance is calculated from a model of a single chip, assuming that the chip bottom surface is isothermal. Second, the thermal resistance is calculated from a chip and submount model, assuming that the submount bottom surface is isothermal. The submount thermal resistance is obtained by subtracting the chip resistance from this combined resistance. The heatsink and the stem thermal resistances are obtained similarly by adding each component to the model and by shifting the isothermal surfaces from the heatsink side facing the stem to the standard outermost patches of the stem. Figure 3(a) shows the result of the self thermal resistance divided into four components. The chip thermal resistance accounts for almost 60% and is the most thermally dominant factor. This is because the chip is the nearest component to the heat source, so the heat flux cannot enter with sufficient spreading, and it has the lowest thermal conductivity. The submount thermal resistance is the second most dominant factor, because

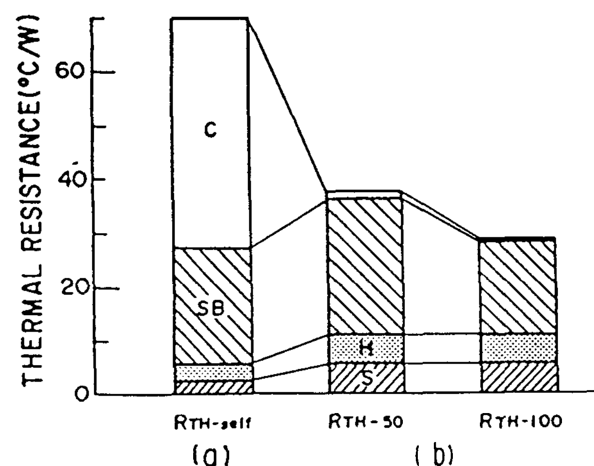

Fig. 3. Distributions of (a) self thermal resistance ($R_{TH\text{-}self}$) and (b) interactive thermal resistance for 50-μm-spaced double-sided element operations ($R_{TH\text{-}50}$) and for 100-μm-spaced double-sided element operations ($R_{TH\text{-}100}$).

the submount is the second nearest component to the heat source.

3.2 *Interactive thermal resistance*

The interactive thermal resistance is divided into four model components similar to the division of the self thermal resistance. Two interactive thermal resistances are considered: one is $R_{TH\text{-}50}$ for 50-μm-spaced double-sided element operations, and the other is $R_{TH\text{-}100}$ for 100-μm-spaced double-sided element operations. The distributions of $R_{TH\text{-}50}$ and $R_{TH\text{-}100}$ are shown in Fig. 3(b). The submount thermal resistance accounts for 60 to 70% of both the $R_{TH\text{-}50}$ and the $R_{TH\text{-}100}$. The chip thermal resistance is the smallest since the lateral heat flow that causes thermal interaction spreads in the high-conductive submount rather than in the low-conductive chip. Furthermore, $R_{TH\text{-}50}$ corresponds to more than 50% and $R_{TH\text{-}100}$ corresponds to about 40% of the self thermal resistance. Therefore, the total interactive thermal resistance of the iter element for four other element operations, the sum of $R_{TH\text{-}50}$ and $R_{TH\text{-}100}$, is comparable to the self thermal resistance. The interactive thermal resistance will increase with an increase in laser element density, making the reduction in interactive thermal resistance as important as self thermal resistance in improving overall laser array thermal performance.

3.3 *Upward and down ward routes thermal resistance*

Two different heat flow routes, shown in Fig. 4(a), contribute to the self thermal resistance. One is the upward route which transmits heat over the bottom surface of each groove, and the other is the downward route which transmits heat under the each groove. The downward route thermal resistance is calculated using a model which only considers the part of the chip below the level of the bottom surfaces of the grooves. The upward route thermal resistance is a parallel resistance to the wnward route resistance.

The downward route thermal resistances of the heatsink and the stem are nearly equal to their standard combined resistances respectively, because the submount can compensate for the heat spreading decrease caused by the absence of the upward heat route. The upward and downward route self thermal resistances in the chip and the submount are shown in Fig. 4(b). The upward route thermal resistance is larger than the downward route by 5.4 times in the chip and 2.6 times in the submount. The upward route cannot transmit heat flux as easily as the downward route, where the flux can directly enter the submount; therefore, the dominant heat flow route is the downward route. Thus, reducing the downward route resistance is a very effective way of reducing the chip thermal resistance.

On the other hand, the parallel connection of the upward and downward route resistances reduces the self thermal resistance almost 20% in the chip and 30% in the submount. Thus, because the upward route is so effective for dividing the heat flow, it is possible to reduce the chip and submount self thermal resistances, which are dominant factors. Moreover, the thermal interactions are caused by heat in the chip moving upward over the grooves and in the submount moving under the grooves, so the interactive thermal resistance can be reduced by adding a medium which can transfer the upward route heat flow to the isothermal surface (this will be discussed further in §4.3).

§4. Improvement in Thermal Resistance

As described in §3, laser array thermal performance can be improved by reducing the dominant chip and submount thermal resistances, by using the upward and downward heat routes. Thus, three areas are targeted for improvement: the submount, the chip, and the interactive thermal resistances. This section gives a detailed description of how to improve these three resistances and the implications for laser array structures. The results are shown in Fig. 5.

4.1 *Submount thermal resistance*

Reducing the submount thermal resistance effectively improves the self and interactive thermal resistances (Fig. 5(a)). They can be reduced by using a submount that is more conductive than standard Si to remove heat more effectively. The dependence of thermal resistance on the submount conductivity is shown in Fig. 6 for the conductivity range from Si to type IIa diamond. The self and in-

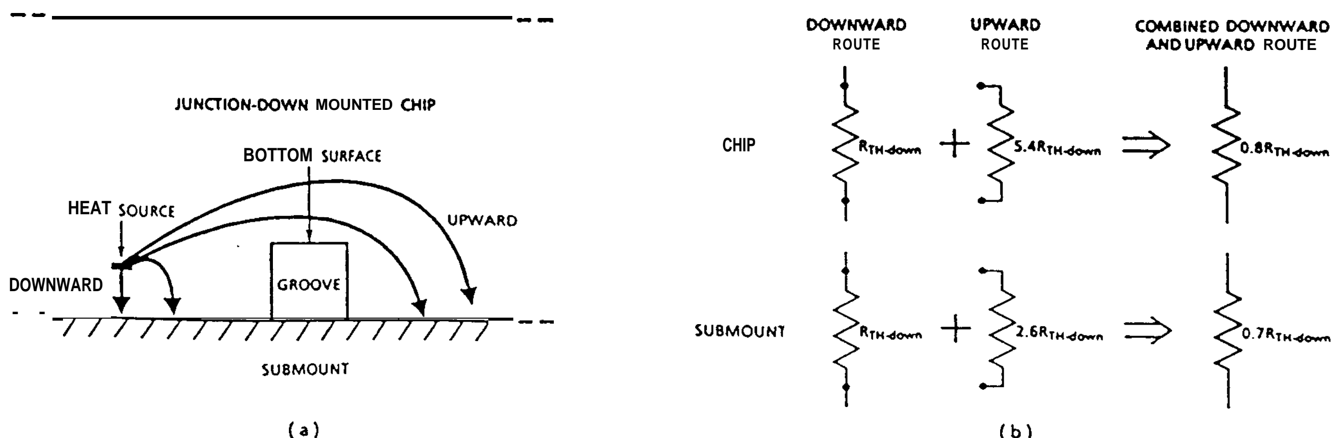

Fig. 4. (a) Upward and downward heat flow routes in the junction-down mounted laser array chip. (b) Dependence of the chip and submount thermal resistance on the two parallel heat flow routes. $R_{TH\ down}$ represents the downward route thermal resistance.

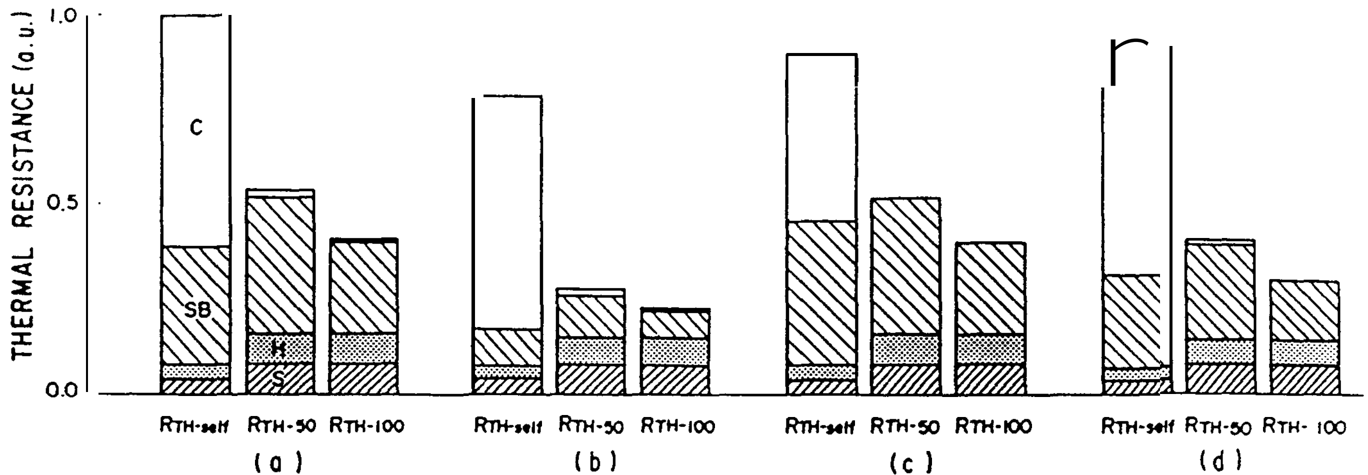

Fig. 5. Distributions of self and interactive thermal resistances for (a) a standard model, (b) a model using a high thermal conductive cBN submount, (c) a model with a thinner (3-μm) cap layer and (d) a model with a heat-pass-wire added as a bypass.

teractive thermal resistances show almost the same dependence on submount conductivity. The submount thermal resistance is reduced by increasing its conductivity, especially when a relatively low conductive submount is used. The heatsink thermal resistance is also reduced because a high-conductive submount can spread the heat flux flowing into the heatsink. The improved thermal resistances of these components account for most of the total interactive thermal resistance (Fig. 5(a)). Therefore, a high-conductive submount is more effective in reducing interactive thermal resistance than self thermal resistance.

Type Ha diamond has the highest conductivity, which is 12 times that of Si. However, it is less practical as a submount because it is only commercially available in sizes so small that its electrode separation yield is low. Recently, SiC and AIN have been commercially used as high-conductive submounts, and cBN, a higher conductive material (3.6 times that of Si), is being developed. As can e seen in Fig. 6, the cBN submount reduces the self and the interactive thermal resistances by about 70% in the submount and about 10% in the heatsink. In total, the cBN submount improves the self thermal resistance by more than 20% and the interactive thermal resistance by nearly 50%. The distribution of its thermal resistance is also shown in Fig. 5(b).

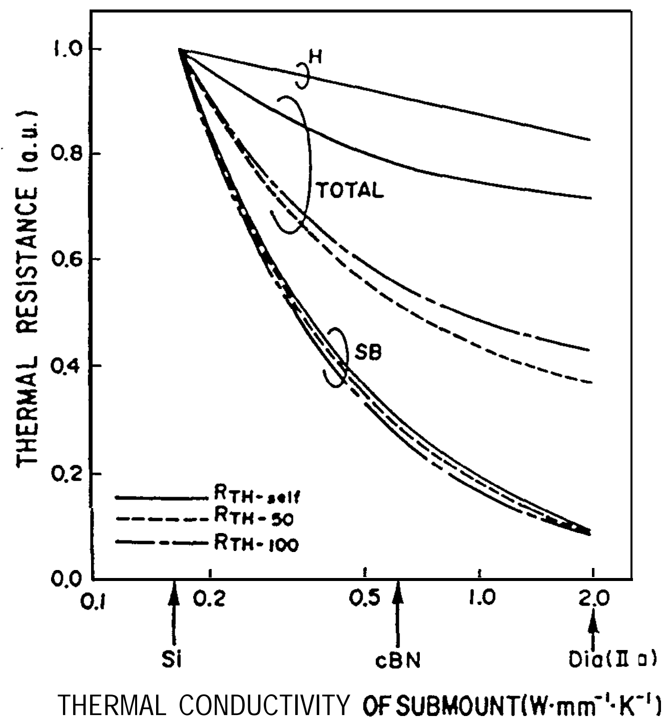

Fig. 6. Dependence of thermal resistance on submount thermal conductivity.

4.2 *Chip thermal resistance*

It is important to reduce the chip thermal resistance since it accounts for almost 60% of the self thermal resistance (Fig. 5(a)), and it becomes even more dominant when a higher conductive submount is used (Fig. 5(b)). This section examines the effect of using a thinner cap layer to utilize the downward route heat flow. Figure 7 shows the dependence of thermal resistance on cap layer thickness for the range from the standard 7 μm to 3 μm. Self thermal resistance in the chip decreases when the thickness of the cap layer is reduced, since the heat source becomes nearer the submount. This tendency becomes stronger as the cap layer becomes thinner. On the other hand, self thermal resistance increases in the submount because the heat flux enters the submount without spreading sufficiently through the chip. However, a thin cap layer can improve the total self thermal resistance since the dominant chip thermal resistance is reduced. Interactive thermal resistance is not improved since only the chip thermal resistance, which is only a small part of the total, is reduced.

As can be seen in Fig. 7, the 3-μm-thick cap layer reduces self thermal resistance in the chip by nearly 30%, but increases it in the submount by more than 20%. Consequently, the total reduction in self thermal resistance is about 10%. The high-conductive submount would be effective against the resistance rise in the submount. Moreover, because the downward route thermal resistance is reduced, the upward route resistance in the chip rises to 9.2 times that of the downward route resistance. Therefore, the heat flux entering the submount through the upward route and through other elements, decreases. This considerably reduces the in-

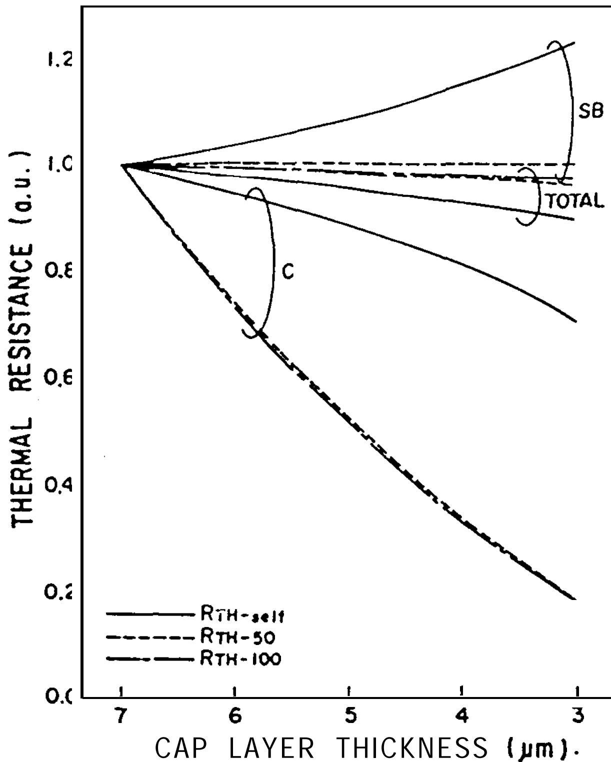

Fig. 7. Dependence of thermal resistance on cap layer thickness.

teractive thermal resistance in the chip by more than 80%. However, because other components cannot be reduced, the total interactive thermal resistance is improved by only 3%. The distribution of its thermal resistance is also shown in Fig. 5(c).

4.3 *Interactive thermal resistance*

To improve interactive thermal resistance, a structure reducing the heat flux entering the submount through other elements is examined. Suppression of the upward eat flow in the chip increases self thermal resistance (Fig. 4(b)). Therefore, a new laser structure is proposed having a medium that can transmit the upward heat flux, thus preventing the heat flow through other elements from causing thermal interactions. Figure 8 shows the structure containing a medium called a heat-pass-wire. The heat-pass-wire uses metal to connect the chip top surface (common electrode side) to the submount top surface that has isolated electrodes for the heat-pass-wire and each of five elements. The submount width is doubled to 2.4 mm, expanding the contact area between the heat-pass-wire and the submount. However, thermal resistance cannot be reduced only by doubling the submount width; the heat-pass-wire must also be added. Here, Cu is used as a heat-pass-wire, since it is a conventional material and has relatively high thermal conductivity (8.7 times that of GaAs).

The thermally optimal shape of this structure is determined by investigating the dependence of the heat-pass-wire effect on chip thickness T_C, heat-pass-wire thickness T_H, thickness H defined in Fig. 8, and distance W between the chip and heat-pass-wire on the submount as shown in Fig. 9. The overall thermal resistance represents the center element thermal resistance including the interactive thermal resistances for the other four element operations. The standard structure dimensions are assumed to be $T_C=60$ μm, $T_H=250$ μm, $H=50$ μm, and $W=100$ μm. The heat-pass-wire effect depends most strongly on parameter T_C. The overall thermal resistance is reduced by thinning T_C, since reducing the distance between the source and the heat-pass-wire reduces the self thermal resistance by improving the upward heat route resistance and the interactive thermal resistance by reducing the heat flux entering the submount through other elements. However, a thinner chip is more difficult to handle. The heat-pass-wire effect also depends on T_H. The overall thermal resistance is reduced by increasing T_H since a thick heat-pass-wire can dissipate the heat flux, thus reducing the heat pass route thermal resistance. However, this effect tends to saturate. Although the overall thermal resistance increase is proportional to W, a three-fold increase in W only produces a 1% increase in overall thermal resistance. A heat-pass-wire of $H=0$, shown by a dashed line in Fig. 9, improves the overall

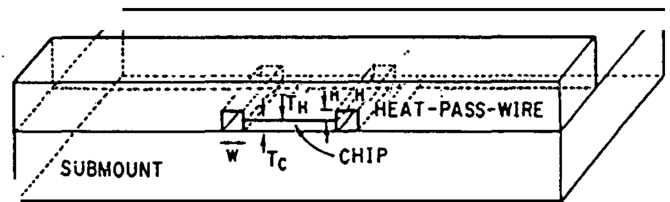

Fig. 8. Heat-pass-wire structure. A chip and a double width submount are also shown.

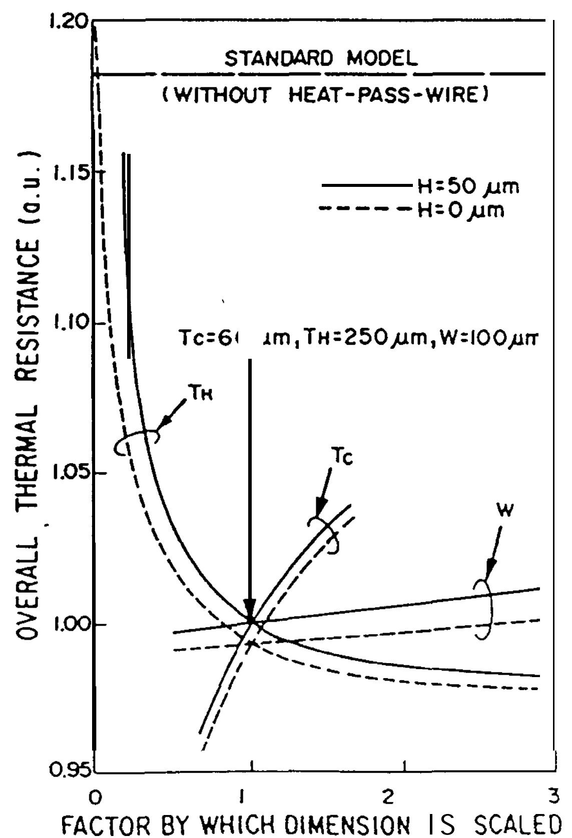

Fig. 9. overall thermal resistance for all element operations as a function of changes in characteristic parameters. T_C: chip thickness, T_H: heat-pass-wire thickness, H: *thickness* defined in Fig. 8, W: distance between the chip and the heat-pass-wire on the submount.

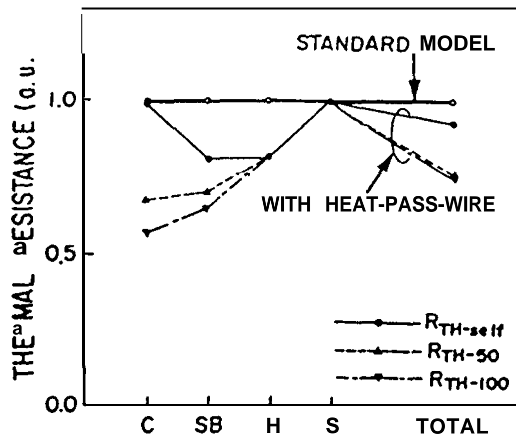

Fig. 10. Effect of heat-pass-wire addition.

thermal resistance by less than 1% when the other dimensions are similar to the standard. Thus, the standard structure shape with the heat-pass-wire is appropriate for a practical thermal design.

Figure 5(d) shows the distribution of thermal resistance for the standard structure with the heat-pass-wire, and Fig. 10 shows the same results normalized for the standard model without the heat-pass-wire. The additional heat-pass-wire reduces interactive thermal resistance by about 30% in the submount and by nearly 20% in the heatsink. It also reduces self thermal resistance by almost 20% in the submount and in the heatsink. This compensates for the rise in the submount self thermal resistance caused by the thin cap layer structure.

4.4 *Overall thermal resistance*

The combined effect of these three structures, a cBN submount, 3-μm-thick cap layer, and heat-pass-wire, is that self thermal resistance, $R_{TH\text{-}50}$, and $R_{TH\text{-}100}$ are reduced by 38%, 56%, and 51%, respectively. Thus, the new compound structure can almost halve the center element's overall thermal resistance for all element operations.

§5. Conclusion

The thermal resistance of a 50-μm-spaced 5-beam laser diode array was calculated for a 3-dimensional practically scaled model, using the Boundary Element Method. The dominant components in reducing self thermal resistance were the chip and the submount. The dominant component in reducing interactive thermal resistance was the submount. When all elements were in operation, the interactive thermal resistance of the center element became comparable to the self thermal resistance. Three structures to improve thermal resistance were examined: (1) A high thermal conductive submount can reduce both the self and the interactive thermal resistances in the submount and the heatsink. (2) A thinner cap layer can reduce the self thermal resistance, but has almost no effect on reducing the interactive resistance. (3) Adding a heat-pass-wire can reduce both the self and the interactive thermal resistances in the submount and the heatsink. The combined effect of these three structures can almost halve the center element's overall thermal resistance for all five element operations.

Total heat source distribution, including such other sources as the radiative transfer of energy, as well as strict layered structure of the chip should be taken into consideration for more rigorous analysis; the heat source consideration will decrease the thermal estimation and the other will increase it.

Acknowledgments

The authors would like to thank Dr. Kiyoshi Itao for encouragement and support. The authors are also indebted to Shigeji Hara and his colleagues for their fruitful discussions on laser structures.

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