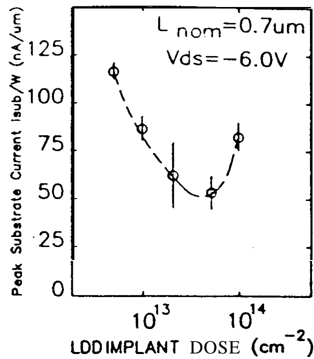

Fig. 4. Dependence of peak substrate currents at $V_{ds} = -6$ V in 0.7-μm gate-length LDD surface-channel PMOSFET's, on the dose of the LDD implant (BF_2 at 50 keV).

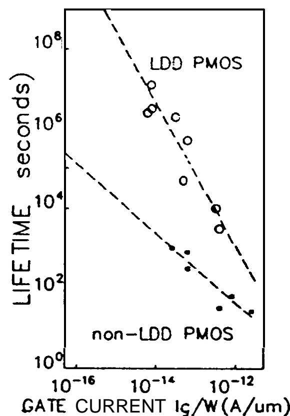

Fig. 5. Comparison of the lifetimes based on 10-mV shift in V_{ts} for non-LDD ($p^- = 5 \times 10^{13}$ cm^{-2}) and LDD surface-channel PMOSFET's, as a function of initial gate current in the stressed condition.

At a channel length of 0.5 μm, the additional series resistance of the p^- extensions in the optimum device (p^- dose of 5×10^{13} cm^{-2}) causes a 9.5-percent reduction in the saturated drain current (i.e., I_{ds} at $V_{gs} = V_{ds} = -5.0$ V) when compared to the non-LDD design.

Fig. 5 compares the lifetime of the optimized LDD PMOSFET with that of the non-LDD devices. The lifetime in this case is again based on a 10-mV shift in V_{ts} and is plotted against the initial gate current under stress. It can be seen that the LDD structure raises the 5-' fetime of these submicrometer surface-channel MOS-FE' n 14 h to well in excess of 10 years.

IV. Conclusions

Hot-electron-induced punchthrough is found to limit the lifetime of 0.8-μm gate-length ($L_{eff} = 0.5$ μm) surface-channel PMOSFET's. Even though these devices are more reliable than conventional buried-channel PMOSFET's, for satisfactory reliability at 5-V operating voltages it is found necessary to adopt a lightly doped drain (LDD) design.

References

[1] G. J. Hu and R. H. Bruce, "Design tradeoffs between surface- and buried-channel FET's," *IEEE Trans. Electron Devices*, vol. ED-32, p. 584, 1985.
[2] S. J. Hillenius, R. Liu, G. E. Georgiou, R. L. Field, D. S. Williams, A. Kornblit, D. M. Boulin, R. L. Johnston, and W. T. Lynch, "A symmetric submicron CMOS technology," in *IEDM Tech. Dig.*, p. 252, 1986.
[3] M. Koyanagi, A. G. Lewis, J. Zhu, R. A. Martin, T. Y. Huang, and J. Y. Chen, "Investigation and reduction of hot electron induced punchthrough (HEIP) effect in submicron PMOSFET's," in *IEDM Tech. Dig.*, p. 722, 1986.
[4] Y. Hiruta, K. Maeguchi, and K. Kanzaki, "Impact of hot electron trapping on half micron PMOSFETs with P+poly gate," in *IEDM Tech. Dig.*, p. 718, 1986.
[5] M. P. Brassington and R. R. Razouk, "The relationship between gate bias and hot-earner-induced instabilities in buried- and surface-channel PMOSFET's," *IEEE Trans. Electron. Devices*, vol. 35, p. 320, Mar. 1988; see also *Tech. Dig. 1987 Symp. VLSI Technol.*, p. 55, May 1987.
[6] A. E. Schmitz, P. K. Vasudev, and J. Y. Chen, "High performance sub-half-micrometer p-channel transistors for CMOS VLSI," in *IEDM Tech. Dig.*, p. 423, 1984.
[7] J. J. Tzou, C. C. Yao, R. Cheung, and H. W. K. Chan, "Hot-carrier-induced degradation in p-channel LDD MOSFET's," *IEEE Electron Device Left.*, vol. EDL-7, p. 5, 1986.

Thermal Analysis of Solid-State Devices Using the Boundary Element Method

CHIN C. LEE, ARTHUR L. PALISOC, AND JOHN M. W. BAYNHAM

Abstract—Thermal analysis of two-dimensional and three-dimensional two-layer device structures have been carried out using the boundary element method (BEM). The resulting thermal profiles agree very well with those obtained using analytical solutions. This agreement indicates not only the accuracy of the BEM but also the correct derivation of the analytical solutions.

I. Introduction

Thermal analysis methods can be categorized into two general approaches, namely, analytical and numerical. The analytical approach involves the search for an exact analytical solution for structures with regular geometries. Solutions for several cyclindrical and rectangular geometries have been derived and applied to various solid-state devices such as laser diodes [1], transistors, device packages [2], and integrated circuits [3].

As to the numerical approach, some works on the thermal analysis of devices have been carried out using finite-difference [4] and finite-element techniques [5]. However, no work on thermal analysis using the boundary element method (BEM) has been reported. The advantages of using BEM include, among other things, the discretization of only the boundary surfaces of the body, the facility with which "surfaces at infinity" can be represented [6], and the simplicity of input data preparation. In this brief, we report the thermal analysis of solid-state devices performed using a BEM software package, BEASY [7], and its comparison with the results obtained using analytical solutions.

II. Analysis of Specific Device Structures and Their Comparison with Analytical Results

Analytical solutions of complicated heat-transfer geometries do not generally exist, and hence, numerical techniques, preferably

Manuscript received February 4, 1988. This work was supported by the University of California MICRO Program with matching funds from Rockwell International and a grant of CPU time on a Cray X-MP/48 Computer from the NSF-supported University of California at San Diego Supercomputer Center.

C. C. Lee and A. L. Palisoc are with the Electrical Engineering Department, University of California, Irvine, CA 92717.
J. M. W. Baynham is with Computational Mechanics, Ashurst Lodge, Ashurst, Southhampton 504 2AA, United Kingdom.

IEEE Log Number 8820829.

0018-9383/88/0700-1151$01.00 ©1988 IEEE

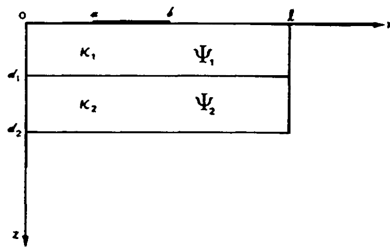

Fig. 1. Double-layer FET thermal model.

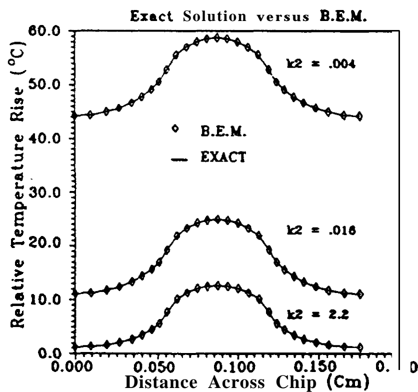

Fig. 2. Thermal profile over the surface of the FET shown in Fig. 1 for three different bonding layer conductivities: 004, 0.016, and 2.2 W/cm-°C.

those that do not involve tedious data preparation, must be used. As a verification to the numerical methods employed, one can compare the results from known analytical solutions with those obtained using the numerical method.

Consider the two-dimensional problem of an FET device as shown in Fig. 1. Here we have a double-layer problem with differing thermal conductivities. A strip heat source with power being uniformly dissipated over it is located on the surface. An isothermal base, heat-sunk to a temperature of 0°C, is assumed. Heat loss is negligible through the edges and through the top surface except where the heat source is located. The analytical solution to this problem can be found in the literature [1]. Fig. 2 shows the thermal profile over the FET device that consists of GaAs and three different bonding layer conductivities. The parameters for this particular problem are detailed in Table I.

The profiles shown in Fig. 2 were calculated using both the BEM and the analytical solution. It is seen here that the two results are virtually identical. Fig. 3 shows the normal component of the heat flux across the GaAs-bonding layer interface. This again shows the excellent agreement between BEM and the analytical solution. The analytical heat flux equation at the interface is obtained by taking the negative of the gradient of the temperature solution and multiplying by the thermal conductivity.

Fig. 4 shows the corresponding three-dimensional two-layer problem of a GaAs chip on an alumina package. The parameters of this configuration are given in Table II, and the boundary conditions are the same as those for the previous two-dimensional problem. Fig. 5 shows the resulting thermal profiles over the chip surface passing through the center of the heat source. The solid line is the profile calculated using the analytical solution [3], and the centered symbols give the profile analyzed with BEM. R is seen that these two profiles are virtually identical. This once again indicates the accuracy of BEM and the correct derivation of the analytical solution. In principle, we should always use analytical solutions to gauge the accuracy of numerical methods. On the other hand, for complicated problems, the derivation of analytical solutions takes several tens of pages to finish. Any minor error would render the final form of the solution useless. The same situation

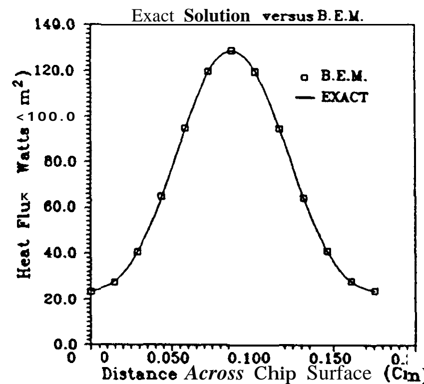

Fig. 3. Normal heat flux at the GaAs-bonding layer interface of the FET device of Fig. 1. The bonding layer conductivity is 2.2 W/cm-°C.

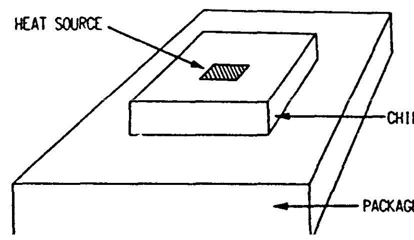

Fig. 4. Typical integrated circuit chip on a package.

TABLE I
KEY PARAMETERS OF THE TWO-DIMENSIONAL DOUBLE-LAYER STRUCTURE

Layer	Top Layer	Bonding Layer
Material	GaAs	Epoxy, Silver-epoxy, Au-Sri preform
Conductivity (Watt/cm-°C)	0.46	.004, .016, 2.2
Thickness (mils)	15	1
Width (mils)	69	69

Heat source: 25 mils wide
Heat flux density over source: 194 watts/cm²

TABLE II
KEY PARAMETERS OF THE THREE-DIMENSIONAL DOUBLE-LAYER STRUCTURE

	First Layer	Second Layer
Material	GaAs	Alumina
Conductivity (Watt/cm-°C)	0.46	0.25
Thickness (mils)	15	15
Size (mil x roil)	50 x 50	50 x 50

Heat source size: 50 microns x 50 microns
Total power over source: 100 mwatt

also applies when the solution is written into a computer program. Thus, in practice, the numerical method may also serve as a helpful indicator as to whether the solution is derived correctly.

III. SUMMARY

We have demonstrated the utility and simplicity of the boundary element method in dealing with the steady-state thermal analysis of solid-state devices. Two device structures have been studied

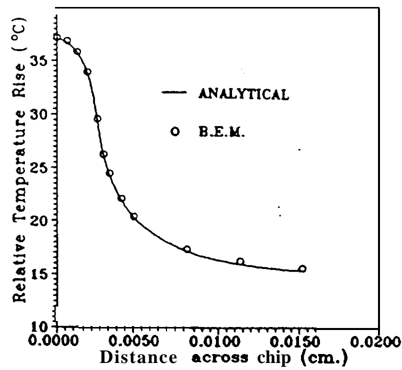

Fig. 5. Thermal profile over the chip surface. The chip and package lateral dimensions are the same: 50 mil x 50 roil.

using both the BEM and the corresponding analytical solutions. It was shown that the agreement between BEM and the analytical solutions is excellent.

The most appealing feature of BEM is the simplicity and ease of data preparation coupled with the fact that it admits discontinuous shape functions for its (boundary) elements. This provides the engineer an invaluable tool for determining the regions in the device model where the mesh needs further refinement. As to the [illegible]y of the method, it must be pointed out that the method mo[illegible] the boundary value problem *exactly* within the domain. Errors are introduced only because we are not able to perform the integrations in closed form but must resort to brute force numerical techniques.

References

[1] W. B. Joyce and R. W. Dixon, "Thermal resistance of heterostructure lasers," *J. Appl. Phys.*, vol. 46, pp. 855–862, Feb. 1975.

[2] G. N. Ellison, "The thermal design of an LSI single-chip package" *IEEE Trans. Parts, Hybrids, Packaging*, vol. PHP-12, pp. 371–378, Dec. 1976.

[3] C. C. Lee and A. L. Palisoc, "Thermal analysis of GaAs integrated circuit devices," in *IEEE GaAs IC Symp. Tech. Dig.* (Grenelefe, FL, Oct. 28–30, 1986), pp. 115-118.

[4] L. M. Mahalingam, J. A. Andrews, and J. E. Drye, "Thermal analysis on pin grid array packages for high density LSI and VLSI logic circuits," *IEEE Trans. Components, Hybrids, Manufact. Technol.*, vol. CHMT-6, pp. 246–256, Sept. 1983.

[5] D. L. Waller, L. R. Fox, and R. J. Hannemann, "Analysis of surface mount thermal and thermal stress performance," *IEEE Trans. Components. Hybrids, Manufact. Technol.*, vol. CHMT-6, pp. 257–266, Sept. 1983.

[6] [illegible] Brebbia, *The Boundary Element Method for Engineers.* Lon- Pentech, 1984.

[illegible] BEASY Software Package, Computational Mechanics, 17744 Skypark Circle, Suite 265, Irvine, CA 92714.

Consideration of Doping Profiles in MOSFET Mobility Modeling

THOMAS J. KRUTSICK AND MARVIN H. WHITE

***Abstract*—Process and device modeling are important for the advancement and development of new technologies. The channel mobility of a MOSFET in the strongly inverted, linear regime is an important parameter in this modeling process and depends upon the effective normal electric field. We show the general form of this field is $E_{eff} = (\eta Q_c + \zeta Q_b)/\epsilon_{Si}$ where Q_c and Q_b are the inversion and bulk charge areal densities, respectively, and the coefficients η and ζ determine the weighting of these charge densities. Previous authors have developed a universal mobility-effective field curve for n-channel MOSFET devices with $\eta = 1/2$ and $\zeta = 1$. Recently, a study of p-channel MOSFET transistors indicates $\eta \approx 1/3$ and $\zeta = 1$, which would seem to imply the inversion charge contribution is different for electrons and holes in MOSFET's. However, we show theoretically, by quantum mechanical arguments, that $\eta = 1/2$ for both n- and p-channel MOSFET's, and the coefficient of the bulk charge contribution ζ depend upon the doping profile in the near-surface region. A uniform doping profile produces a value of $\zeta = 1$, while a nonuniform profile near the interface leads to $\zeta > 1$ (accumulation) or $\zeta < 1$ (depletion). We provide experimental results to support these conclusions.**

Manuscript received July 7, 1987; revised February 10, 1988. This work was supported by the Office of Naval Research under Contract N000 14-86-K-04 11, by the Hewlett-Packard Foundation, and by the Fairchild Foundation.

The authors are with the Sherman Fairchild Center, Lehigh University, Bethlehem, PA 18015.

IEEE Log Number 8820823.

I. Introduction

The accurate modeling of cat-tier mobility in MOSFET inversion layers is required for the prediction of device performance, the guidance of process technology, and the study of surface transport. The electron mobility has been found to follow a "universal curve independent of substrate bias when plotted as a function of the effective normal electric field [1], [2]. Recently, a universal curve for p-channel transistors has been proposed with an effective normal field different from the n-channel case [3], [4]. This effective field is generally given by

$$E_{eff} = \frac{1}{\epsilon_{Si}} (\eta Q_c + \zeta Q_b) \quad (1)$$

where Q_c and Q_b are the channel and bulk surface charge densities, respectively. The purpose of this brief is to consider the doping profile effect upon the mobility-field relationship.

II. Theory

If we consider surface roughness as the dominant degradation mechanism at high normal electric fields and take into account the two-dimensionality of the channel, then we can show that the high-field mobility varies with the effective normal field as [5]

$$E_c = \frac{\int_0^\infty dx\, N_i |\Psi_i(x)|^2 E(x)}{\int_0 dx\, N_i |\Psi_i(x)|^2} = \left(\eta Q_c + \left(1 - \frac{\bar{x}}{W}\right) \zeta Q_b\right) \Big/ \epsilon_{Si} \approx \frac{\eta Q_c + \zeta Q_b}{\epsilon_{Si}} \quad (2)$$

where N_i is the carrier concentration of the ith subband, Ψ_i is the wave function describing the carriers of the ith subband, $E(x)$ is the electric field in the direction normal to the surface, $\bar{x}$ is the centroid of the inversion layer distribution, and W is the depletion layer width ($\bar{x} \ll W$). Assuming either a triangular potential well with Airy function solutions or a Stem-Howard [6] variational wavefunction[1] for the case of uniform doping gives $\eta = 0.5$ and $\zeta = 1.0$ [7]. If we consider a bulk doping profile represented by the constant N_b, except for a small region near the surface depicted by the constant N_s which extends from the surface to a depth of several inversion layer thicknesses, then it can be shown that

$$\zeta \approx \left(1 \pm \frac{N_s - N_b}{N_b}\right) = 1 \pm \frac{\Delta Q_s}{Q_b} \quad (3)$$

[1] The Stem-Howard wavefunction is applicable only for the lowest subband (i.e., $i = 0$).

0018-9383/88/0700-1153$01.00 ©1988 IEEE